AMENDMENTS TO THE CLAIMS

This listing of claims will replace all prior versions, and listings, of claims in the application.

Listing of Claims:

1. (Currently Amended) A receiving apparatus comprising:

at least one ~~or more~~ variable gain ~~amplifiers~~amplifier;

at least one ~~or more~~ level detection ~~circuits, at least one~~circuit, which detects at least one ~~or more levels~~level output from said at least one ~~of the~~ variable gain amplifier ~~or amplifiers~~;

at least one ~~or more~~ comparing ~~circuits~~ circuit for comparing ~~to~~ at least one ~~or more~~ reference ~~levels~~ level to said at least one ~~or more outputs~~ output from said at least one ~~of the~~ level detection circuit ~~or circuits~~;

at least one ~~or more demodulators~~demodulator;

at least one ~~or more~~ binarizing ~~circuits~~circuit;

at least one ~~or more~~ gain switching detection ~~circuits~~ circuit detecting switching of at least one ~~or more gains~~gain of said at least one ~~of the~~ variable gain amplifier ~~or amplifiers~~;

at least one ~~or more~~ slice level holding ~~circuits~~ circuit holding at least one ~~or more~~ substantially constant ~~values~~ value at least one ~~or more~~ slice ~~levels~~ level employed by said at least one ~~of the~~ binarizing circuit ~~or circuits~~; and

at least one ~~or more~~ counter ~~circuits~~circuit;

wherein at least one gain of said at least one ~~of the~~ variable gain amplifier ~~or amplifiers~~ is switched based on at least one result of comparison by said at least one ~~of the~~ comparing circuit ~~or circuits~~; and

wherein, when switching of said at least one ~~of the~~ gain ~~or gains~~ is detected by said at least one ~~of the~~ gain switching detection circuit ~~or circuits~~, said at least one ~~of the~~ counter circuit ~~or circuits~~ and said at least one ~~of the~~ slice level holding circuit ~~or circuits cause~~ causes said at least one ~~of the~~ slice level ~~or levels~~ to be held at said at least one ~~of the~~ substantially constant value ~~or values~~ for at least one ~~or more~~ prescribed ~~times~~time.

2. (Currently Amended) ~~A~~ The receiving apparatus according to claim 1 ~~in which~~, wherein said at least one ~~of the~~ variable gain amplifier ~~or amplifiers also~~ serves as at least one bandpass filter.

3. (Currently Amended) ~~A~~ The receiving apparatus according to claim 1 ~~in which~~, wherein said at least one ~~of the~~ comparing circuit ~~or circuits also~~ serves as at least one gain switching detection circuit.

4. (Currently Amended) ~~A~~ The receiving apparatus according to claim 1 ~~in which~~, wherein said at least one time counted by said at least one ~~of the~~ counter circuit ~~or circuits~~ is variable.

5. (Currently Amended) ~~A~~ The receiving apparatus according to claim 1 ~~in which~~, wherein said at least one ~~of the~~ binarizing circuit ~~or circuits~~ comprises:

at least one ~~or more~~ minimum value detection ~~circuits~~ circuit and at least one ~~or more~~ maximum value detection ~~circuits~~ circuit accepting input of at least one ~~or more~~ demodulated ~~signals~~ signal from said at least one ~~of the~~ demodulator ~~or demodulators~~ by way of at least one ~~or more~~ demodulated signal holding ~~circuits~~ circuit and respectively detecting at least one ~~or more~~ minimum ~~values~~ value and at least one ~~or more~~ maximum ~~values~~ value of said at least one ~~of the~~ demodulated signal ~~or signals~~ input thereto;

at least one ~~or more~~ adding ~~circuits~~ circuit adding said at least one ~~of the~~ minimum value ~~or values~~ and said at least one ~~of the~~ maximum value ~~or values~~;

at least one ~~or more amplifiers~~ amplifier substantially halving at least one output of said at least one ~~of the~~ adding circuit ~~or circuits~~; and

at least one ~~or more~~ comparing ~~circuits~~ circuit carrying out binarization by comparing at least one magnitude of at least one

output from said at least one ~~of the~~ amplifier ~~or amplifiers~~ and at least one magnitude of said at least one ~~of the~~ demodulated signal ~~or signals~~ from said at least one ~~of the~~ demodulator ~~or demodulators~~;

said at least one ~~of the~~ demodulated signal holding circuit ~~or circuits~~ functioning as said at least one ~~of the~~ slice level holding circuit ~~or circuits~~.

6. (Currently Amended) ~~A~~ The receiving apparatus according to claim 1 ~~in which~~, wherein said at least one ~~of the~~ binarizing circuit ~~or circuits~~ comprises:

at least one ~~or more~~ offset canceler ~~circuits~~ circuit outputting, when at least one ~~or more signals~~ signal input thereto is ~~or are~~ less than at least one ~~or more~~ lower cutoff ~~values~~value, said at least one signal corresponding to at least one amount by which said at least one ~~of the~~ signal ~~or signals~~ input thereto is less than said at least one ~~of the~~ lower cutoff value ~~or values~~, ~~and/or~~and outputting, when said at least one ~~or more signals~~signal input thereto is ~~or are~~ greater than said at least one ~~or more~~ upper cutoff ~~values~~value, said at least one signal corresponding to said at least one amount by which said at least one of the signal ~~or signals~~ input thereto is greater than said at least one ~~of the~~ upper cutoff value ~~or values~~;

at least one ~~or more~~ integrating circuits integrating said at least one ~~of the~~ output ~~or outputs~~ therefrom;

at least one ~~or more~~ offset canceler output holding ~~circuits~~ circuit provided between said at least one ~~of the~~ offset canceler circuit ~~or circuits~~ and said at least one ~~of the~~ integrating circuit ~~or circuits~~;

at least one ~~or more~~ adding ~~circuits~~ circuit adding and feeding back at least one ~~or more outputs~~ output from said at least one ~~of the~~ integrating circuit ~~or circuits~~ to at least one ~~or more~~ input ~~signals~~signal; and

at least one ~~or more~~ sign determining ~~circuits~~ circuit using the sign of at least one signal output from said at least one ~~of the~~ adding circuit ~~or circuits~~ to carry out binarization;

said at least one ~~of the~~ offset canceler output holding circuit ~~or circuits~~ functioning as said at least one ~~of the~~ slice level holding circuit ~~or circuits~~.

7. (New) The receiving apparatus according to claim 1, wherein said at least one binarizing circuit or circuits comprises:

at least one offset canceler circuit outputting, when at least one signal input thereto is less than at least one lower cutoff value, said at least one signal corresponding to at least one amount by which said at least one signal input thereto is less than said at least one lower cutoff value, or outputting, when said at least one signal input thereto is greater than said

at least one upper cutoff value, said at least one signal corresponding to said at least one amount by which said at least one signal input thereto is greater than said at least one upper cutoff value;

at least one integrating circuit integrating said at least one output therefrom;

at least one offset canceler output holding circuit provided between said at least one offset canceler circuit and said at least one integrating circuit;

at least one adding circuit adding and feeding back at least one output from said at least one integrating circuit to at least one input signal; and

at least one sign determining circuit using the sign of at least one signal output from said at least one adding circuit to carry out binarization;

said at least one offset canceler output holding circuit functioning as said at least one slice level holding circuit.